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Description

METHOD OF MANUFACTURING A THIN FILM TRANSISTOR OF A LIQUID CRYSTAL DISPLAY

BACKGROUND OF INVENTION

[0001] 1. Field of the Invention

[0002] The invention relates to a method of manufacturing a matrix device, and more particularly, to a method of manufacturing a thin film transistor liquid crystal display (TFT-LCD).

[0003] 2. Description of the Prior Art

[0004] Since the progress of science and technology has led to small, effective, and portable intelligent information products, display devices have played an important role in modern society. In recent years, display devices have undergone great improvements in the areas of high performance quality, larger size, and lower cost. TFT-LCDs have characteristics of thinness, lightness and low power con-

sumption and are expected to have in future a large market as a display device to replace CRTs. It is an important subject to develop a fabrication technique for realizing high achievement and low prices of TFT-LCDs.

[0005] Either for a conventional twist nematic (TN) LCD or for a recently developed wide view angle LCD, such as the IPS-LCD and the MVA-LCD, switch devices are required to control changes of the images. A popularly used switch device, TFT, includes a gate electrode, a source electrode, a drain electrode, and other needed semiconductor or insulating layers. The fabrication process of a TFT substantially decides the total process steps of a whole LCD, so simplifying the fabrication process of the TFT can realize low prices of TFT-LCDs.

[0006] The conventional fabrication method utilizes 5 or 4 masks to achieve a TFT in a liquid crystal display. The necessary elements of a TFT device include a source electrode, a drain electrode, a gate electrode and a channel region. For forming these necessary elements, the regular process steps are required and thus difficult to be omitted. However, with the application of halftone photolithograph making progress, the photo-etching-process can use a single mask to form photoresistors into different thick-

nesses. This makes reduction of the fabrication process possible.

SUMMARY OF INVENTION

[0007] It is therefore a primary objective of the claimed invention to provide a fabrication method of a thin film transistor to solve the above-mentioned problem to simplify the fabrication process thereof.

[0008] According to the claimed invention, a method for fabricating a thin film transistor (TFT) of a liquid crystal display (LCD) includes sequentially depositing a transparent conductive layer, a first metal layer, a first insulating layer, a semiconductor layer, and a second metal layer on a substrate. Following that, a first photo-etching-process (PEP) is performed to remove portions of the second metal layer, the semiconductor layer, the first insulating layer, the first metal layer, and the transparent conductive layer to form a source electrode and a drain electrode and define a channel region. A second insulating layer is deposited followed by performing a second PEP to remove portions of the second insulating layer to form a plurality of contact holes. Finally, a third metal layer is deposited to electrically connect the source electrode and the drain electrode with other wires, and a third PEP is performed to

remove portions of the third metal layer. The first PEP includes a first halftone photolithograph process, and the first halftone photolithograph process forms a first photoresist layer and a second photoresist layer on the second metal layer.

[0009] According to the claimed invention, a method for fabricating a liquid crystal display (LCD) includes sequentially depositing a transparent conductive layer, a first metal layer, a first insulating layer, a semiconductor layer, and a second metal layer on a substrate. Following that, a first photo-etching-process (PEP) is performed to remove portions of the second metal layer, the semiconductor layer, the first insulating layer, the first metal layer, and the transparent conductive layer to form a gate line and a common line and define a TFT region, a channel region and a pixel electrode region. A second insulating layer is deposited followed by performing a second PEP to remove portions of the second insulating layer, the semiconductor layer, the first insulating layer, and the first metal layer to form a plurality of contact holes and expose portions of the transparent conductive layer. Finally, a third metal layer is deposited, and a third PEP is performed to form a data line and a capacitance region and electrically connect

the TFT region and the pixel electrode region. The first PEP includes a first halftone photolithograph process, and the first halftone photolithograph process forms a first photoresist layer and a second photoresist layer on the second metal layer.

[0010] It is an advantage of the claimed invention that the fabrication method can simplify the process steps of the LCD, for example reduce the needed mask number from 4 or 5 to 3. Therefore, the present invention can realize low prices of TFT-LCDs.

[0011] These and other objectives of the present invention will no doubt become obvious to those of ordinary skill in the art after reading the following detailed description of the preferred embodiment that is illustrated in the various figures and drawings.

Brief Description of Drawings

[0012] Fig. 1 is a schematic diagram of a liquid crystal display;

[0013] Figs. 2-7 are schematic diagrams of a fabrication process of a liquid crystal display according to the present invention; and

[0014] Figs. 8-9 are schematic diagrams of another fabrication process of a liquid crystal display according to the present

invention.

DETAILED DESCRIPTION

[0015] Please refer to Fig. 1, which is a schematic diagram of a liquid crystal display (LCD) 10. The LCD 10 comprises a plurality of gate lines 12, a plurality of data lines 14, a plurality of switch devices 16, and a plurality of pixel electrodes 18. Each switch device 16 is connected to a corresponding gate line 12 and a corresponding data line 14, and controls charging the connecting pixel electrode 18.

[0016] Please refer to Figs. 2-7, which explicitly describe the fabrication process of the LCD 10. In the first preferred embodiment, for manufacturing the LCD 10, a transparent substrate 20 is provided. As shown in Fig. 3, a transparent conductive layer 22, a first metal layer 24, a first insulating layer 26, a semiconductor layer 28, and a second metal layer 30 are sequentially deposited on the substrate 20. After the deposition, a first photo-etching-process (PEP) is performed. The first PEP includes a first halftone photolithograph process, and forms two photoresistors having different thicknesses, such as a first photoresistor 32 and a second photoresistor 34. In the first halftone photolithograph process, a mask with slit patterns is irradiated by an electron beam or a laser. The pitches of the

slit patterns are defined corresponding to the wavelength of the electron beam or the laser, and can form different thickness on different portions of the photoresistor layer. After exposing, the photoresisor layer is formed into two different thickness areas, a first photoresistor 32 and a second photoresistor 34. After forming the first photoresistor 32 and the second photoresistor 34, as shown in Figs. 2 and 3, the first PEP further includes a first etching process to remove portions of the second metal layer 30, the semiconductor layer 28, the first insulating layer 26, the first metal layer 24, and the transparent conductive layer 22 and form a gate line 60 and a common line 62. Then, the second photoresistor 34 is removed and a second etching process is performed. Portions of the second metal layer 30 are removed to define a source/drain region 64, a channel region 66 and a pixel electrode region 68.

[0017] Please refer to Figs. 4 and 5. After performing the first PEP, a second insulating layer 36 is deposited and a second PEP is performed. During proceeding the second PEP, a second halftone photolithograph process is performed to form a third photoresistor 38 and a fourth photoresistor 39. The third photoresistor 38 and the fourth photore-

sistor 39 are formed to define the pattern of the second insulating layer 36. Firstly, the second PEP uses a third etching process to remove portions of the second insulating layer 36, the semiconductor layer 28, the first insulating layer 26 and the first metal layer 24 uncovered by the third photoresistor 38 and the fourth photoresistor 39. Then, the fourth photoresistor 39 is removed, and portions of the second insulating layer 36 are removed to form a plurality of contact holes 70. After the second PEP process, portions of the transparent conductive layer 22 are exposed to fit the pattern of the pixel electrode region 68, and two contact holes 70 are formed on the exposed second metal layer 30 in the source/drain region 64.

[0018] Please refer to Figs. 6 and 7. After the second PEP, a third metal layer 40 and a passivation layer 41 are deposited and a third PEP is performed. Firstly, the third metal layer 40, the passivation layer 41 and a fifth photoresistor 42 are formed. Then, a fourth etching process is performed to remove portions of the third metal layer 40 and the passivation layer 41, and form a data line 72, a conduction region 74 and a capacitance region 76. The data line 72 electrically connects the source/drain region 64 through one of the contact hole 70, and the conduction

region 74 conducts the source/drain region 64 and the pixel electrode region 68 through the other contact hole 70 formed in the source/drain region 64. As shown in Figs. 6 and 7, peripheries of the two pixel electrode regions 68 positioned on two sides of the common line 62 and the common line 62 are covered with the second insulating layer 36. The third metal layer 40 strides across the common line 62 to electrically connect the two pixel electrode regions 68. The third metal layer 40 conducts the two pixel electrode regions 68 and forms the capacitance region 76 with the common line 62. In addition, in accordance with the requirements, the third metal layer 40 conducts the first metal layer 24 and the second metal layer 30 at a contact pad 78. The contact pad 78 is electrically connected to a driving circuit, a driving IC or a common voltage.

[0019] The present invention can be also achieved by another process. In the second preferred embodiment, the first PEP is similar to that in the first embodiment, but the second and third PEPs are different.

[0020] Please refer to Fig. 8. After performing the first PEP, a second insulating layer 36 is deposited and a different second PEP is performed. During proceeding the second PEP,

only the third photoresistor 38 is formed to define the pattern of the second insulating layer 36. The second PEP uses a fifth etching process to remove portions of the second insulating layer 36, the semiconductor layer 28, the first insulating layer 26, and the first metal layer 24 uncovered by the third photoresistor 38 or the second metal layer 30. During proceeding the fifth etching process, a chemical solution with high etching selectivity is utilized to remove the first metal layer 24 and retain the second metal layer 30. Because of the chemical characteristics of the first metal layer 24 and the second metal layer 30, the selected solution can be only reacted with the first metal layer 24. After the second PEP, portions of the transparent conductive layer 22 are exposed to fit the pattern of the pixel electrode region 68, and two contact holes 70 are formed on the exposed second metal layer 30 in the source/drain region 64.

[0021] Please refer to Fig. 9. After the second PEP, a third metal layer 40 and a passivation layer 41 are deposited and a third PEP is also performed. Firstly, the third metal layer 40, the passivation layer 41 and a fifth photoresistor 42 are formed. Then, a sixth etching process is performed to remove portions of the third metal layer 40 and the passi-

vation layer 41, and form a data line 72, a conduction region 74 and a capacitance region 76.

[0022] The substrate 20 is on condition that allows light to pass through, such as a glass substrate, a quartz substrate, or a plastic substrate. The transparent conductive layer 22 is an indium tin oxide (ITO) or an indium zinc oxide (IZO). The first metal layer 24, the second metal layer 30 and the third metal layer 40 are composed of tungsten (W), chromium (Cr), aluminum (Al), copper (Cu), molybdenum (Mo),or an alloy of any of the above metals.

[0023] The above-mentioned embodiment is explained with a general TN TFT-LCD, and the claimed fabrication process of other types LCD, such as STN TFT-LCD, IPS TFT-LCD or MVA TFT-LCD, is similar to that of the TN TFT-LCD. In contrast to the prior art, the present invention can simplify the process steps so that can realize low prices of TFT-LCDs.

[0024] Those skilled in the art will readily observe that numerous modifications and alterations of the device may be made while retaining the teachings of the invention. Accordingly, the above disclosure should be construed as limited only by the metes and bounds of the appended claims.